WHAT IS CLAIMED IS:

1. A semiconductor device containing a multi-layered wiring structure formed on a semiconductor substrate, the structure including at least two wiring layers formed in an interlayer insulation layer, and each of the wiring layers including a metal wiring made of one of Cu and a Cu alloy;

wherein the multi-layered wiring structure comprises:

a lower wiring layer formed under the interlayer insulation layer;

a via buried in the interlayer insulation layer to connect an upper wiring layer and the lower wiring layer; and

a dummy via buried in the interlayer insulation layer, the dummy via being not connected to the upper wiring layer.

2. A semiconductor device according to claim 1, wherein the dummy via is buried in the interlayer insulation layer between a dummy wiring layer and the lower wiring layer.

3. A semiconductor device according to claim 1, wherein the dummy via includes Cu buried in a via hole formed in the interlayer insulation layer.

4. A semiconductor device according to claim 1, wherein the lower wiring layer includes at least one damaged region formed at a portion of the lower wiring

layer corresponding to the dummy via buried in the interlayer insulation layer.

5. A semiconductor device according to claim 4, wherein the damaged region includes a region formed by forming the via hole in the interlayer insulation layer.

6. A semiconductor device according to claim 1, wherein the lower wiring layer includes a portion having a width greater than that of a remaining thereof and a plurality of vias are formed in the interlayer insulation film.

7. A semiconductor device according to claim 4, wherein the damaged region is located at a peripheral part surrounding a contact portion of the lower wiring layer contacting with the via.

8. A semiconductor device according to claim 4, wherein the damaged region is located away from the contact portion by a minimum distance defined by a design rule.

9. A semiconductor device according to claim 4, wherein a plurality of damaged regions are formed at portions of the lower wiring layer facing three of four sides of a location contacting with a contact portion of the via.

10. A semiconductor device according to claim 4, wherein the dummy via buried in the interlayer insulation layer includes one end contacting with the

damaged region of the lower wiring layer and the other end which is not connected with the upper wiring layer.

11. A semiconductor device according to claim 10, wherein the dummy via contains a structure similar to that of the via.

12. A semiconductor device according to claim 10, wherein a dummy wiring connected to the dummy via is formed on the interlayer insulation layer as a dummy wiring pattern which is not connected with the via.

13. A semiconductor device according to claim 12, wherein the dummy wiring layer and the upper wiring layer are formed in the same wiring layer.

14. A semiconductor device containing a multi-layered wiring structure formed on a semiconductor substrate, the multi-layered wiring structure including at least two wiring layers formed in an interlayer insulation layer, and each of the wiring layers including a metal wiring made of one of Cu and a Cu alloy;

wherein the multi-layered wiring structure comprises:

a narrow width lower wiring layer connected with a wide width lower wiring layer, the narrow width lower wiring layer and the wide width lower wiring layer being formed in a wiring layer formed in the interlayer insulation layer;

a via buried in the interlayer insulation film to

connect the narrow width lower wiring layer with an upper wiring layer; and

a dummy via buried in the interlayer insulation layer, the dummy via being not connected to the upper wiring layer.

15. A semiconductor device according to claim 14, wherein the dummy via is formed in the interlayer insulation layer at a location corresponding to the damaged region formed in a vacant region between the narrow width lower wiring layer and the wide width lower wiring layer.

16. A semiconductor device according to claim 15, wherein a dummy via contacting with the damaged region is buried in the interlayer insulation layer.

17. A semiconductor device according to claim 14, wherein the dummy via includes a structure similar to that of the via.

18. A semiconductor device according to claim 14, wherein a dummy wiring connected to the dummy via is formed on the interlayer insulation layer as a dummy wiring pattern which is not connected with the via.

19. A semiconductor device according to claim 18, wherein the dummy wiring layer and the upper wiring layer are formed in the same wiring layer.

20. A semiconductor device comprising:

a lower wiring layer formed on a semiconductor substrate using Cu or a Cu alloy;

an interlayer insulation layer formed on the lower wiring layer;

an upper wiring layer formed on the interlayer insulation layer;

a via buried in a via hole formed in the interlayer insulation layer to connect the upper wiring layer and the lower wiring layer having a damaged region formed at a portion corresponding to the via hole; and

a dummy via buried in a dummy via hole formed in the interlayer insulation layer in a similar manner as the via hole, the dummy via being not connected with the upper wiring layer.